Amendments to the Claims

1. (currently amended): A method for forming an ~~a low capacitance~~ isolation tub comprising the steps of:

providing a region of semiconductor material;

forming a plurality of shapes in the region of semiconductor material~~, wherein the shapes are free standing, and wherein adjacent rows of shapes are offset from each other~~; and

exposing the plurality of shapes to an ambient that includes a chemical species that reacts with the plurality shapes to form the low capacitance isolation tub.

2. (original): The method of claim 1 wherein the step of exposing includes thermally oxidizing the plurality of shapes to form a silicon oxide isolation tub.

3. (original): The method of claim 1 further comprising the step of forming a boundary around the plurality of shapes, wherein the boundary includes a recessed portion.

4. (original): The method of claim 1 wherein the step of exposing includes consuming substantially all of the plurality of shapes.

5. (original): The method of claim 1 further comprising the step of forming a passive device over the low capacitance isolation tub.

6. (original): The method of claim 1 wherein the step of forming the plurality of shapes includes etching exposed portions of the region of semiconductor material.

7. (original): The method of claim 6 wherein the step of etching includes etching to a depth from about 6 microns to about 10 microns.

8. (currently amended): The method of claim 1, wherein the step of forming the plurality of shapes includes forming a matrix of free standing shapes, wherein adjacent rows of shapes are offset from each other. ~~6 wherein the step of etching includes reactive ion etching~~.

9. (original): The method of claim 1 wherein the step of providing the region of semiconductor material includes providing a region comprising silicon.

10. (original): A process for forming an integrated circuit device including the steps of:

forming a matrix of shapes within a semiconductor layer, wherein the matrix of shapes comprises offset rows; and

forming a dielectric region within the matrix of shapes.

11. (original): The process of claim 10 wherein the step of forming the matrix of shapes includes forming a matrix of squares.

12. (original): The process of claim 10 wherein the step of forming the dielectric region includes oxidizing the matrix of shapes.

13. (original): The process of claim 12 wherein the step of oxidizing forms a nearly continuous silicon oxide tub.

14. (original): The process of claim 10 further comprising the step of forming a passive component over the dielectric region.

15. (original): The process of claim 10 further comprising the step of forming an isolation trench in the region of semiconductor material.

16. (original): The process of claim 10 further comprising the steps of:

forming a dielectric layer on sidewalls of the matrix of shapes; and

forming a polycrystalline semiconductor layer over the dielectric layer.

17. (original): The process of claim 10 wherein the step of forming the matrix of shapes includes forming a matrix of shapes wherein shapes in a first row have a first spacing, and wherein the shapes in the first row have a second spacing from shapes in a second row, and wherein the second spacing is less than the first spacing.

18. (original): A semiconductor device comprising:

a region of semiconductor material; and

a dielectric tub comprising a matrix of shapes, wherein adjacent rows of shapes are offset.

19. (original): The device of claim 18 wherein the dielectric tub comprises oxidized silicon shapes.

20. (original): The device of claim 18 wherein the dielectric tub includes a boundary having a recessed portion.